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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,611	01/28/2004	Travis Swanson	DB001096-000	3432

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EXAMINER	
CHUNG, PHUNG M	
ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
12/05/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/766,611	SWANSON ET AL.	
	Examiner	Art Unit	
	PHUNG My CHUNG	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7 and 9-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7 and 9-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 May 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/19/08 has been entered.

Claim Rejections - 35 USC § 112

2. Claims 1-2 and 4-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, lines 1-3, "A method of providing a signaling pattern..., said method comprising:

For each selected bit line in said plurality of bit lines, a memory controller:" This claim is a hybrid claim because the preamble of the claim is a method but the body of the claim is a system for example "said method comprising..., a memory controller". Appropriate correction and/or clarification is required.

As per claims 2 and 4-6, these claims are also rejected because they dependent upon the rejected base claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to

> be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-2, 3-7, 9, 20 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (Silvestri (6,385,129)) in view of Cranford, Jr. et al (US 2005/0111536).

As per claims 20 and 23-25, Silvestri discloses a system comprising:

Amemory chip (505);

A bus (511,512) having a plurality of bit lines; and

A processor (502) connected to the memory chip via the bus and a communication therewith through the bus. Silvestri does not perform the following:

select a first group of bit lines from the bus to carry a first plurality of data patterns;

Select at least one of the remaining bit lines from the bus not within the first group to carry a second plurality of data patterns;

Transmit the first plurality of data patterns on the first group of bit lines a selected one of the plurality of bit lines in the bus, and

Transmit the second plurality of data patterns on the at least one of the remaining bit lines one or more of the plurality of bit lines other than the selected bit line. However, the system of Silvestri can perform these method steps (See Fig. 5, col. 5, lines 57-67 to col. 6, lines 1-3). Silvestri does not disclose a serial presence detect circuit containing a plurality of test bits. However, Cranford, Jr. et al disclose a serial presence detect circuit containing a plurality of test bits (an integrated transmission chip (1) may comprise an internal build-in self test unit BIST (1.6) which is able to generate a pseudo random bit sequence PRBS. This bit sequence can be used for further tests). (See paragraph (0066)). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the serial presence detect circuit containing a plurality of test bits (an integrated transmission chip (1) may comprise an internal build-in self test unit BIST (1.6) which is able to generate a pseudo random bit sequence PRBS. This bit sequence can be used for further tests) as taught by Cranford, Jr. et al into the memory chip of Silvestri so that it can be able to generate a pseudo random bit sequence PRBS which can be used for further tests.

As per claims 1-2, 4-7 and 9, these method claims are rejected under similar rationale as set forth in the system claims 20 and 23-25.

5. Claims 10-19 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Silvestri (6,385,129) in view of Cranford, Jr. et al (US 2005/0111536) as applied to claim 20 above, and further in view of Enstrom (5,530,895).

As per claims 21-22, the teaching of Silvestri and Cranford, Jr. et al have been discussed above. Silvestri and Cranford, Jr. et al do not specifically disclose perform a data write/read operation at one of the plurality of storage locations using the bus after each bit in the first and the second plurality of data patterns is transmitted on respective bit lines in the bus. However, Enstrom does disclose perform a data write/read operation at one of the plurality of storage locations using the bus after each bit in the first and the second plurality of data patterns is transmitted on respective bit lines in the bus. (See col. 2, lines 18-88 and col. 5, line 62 to col. 6, line 12). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the step of performing a data write/read operation at one of the plurality of storage locations using the bus after each bit in the first and the second plurality of data patterns is transmitted on respective bit lines in the bus as taught by Enstrom into the invention of Silvestri and Cranford, Jr. et al so that data read out from the memory can be check for errors.

As per claims 10 and 16-18, these claims are rejected under similar rationale as set forth in claim 20-22.

As per claims 11-14 and 19, Silvestri further discloses a strobe signal received from a delay locked loop DLL; Configuring the delay locked loop to

provide a delay to the strobe signal so as to enable latching of the data. (See col. 1, lines 16-25).

As per claim 15, Silvestri and Enstrom do not disclose changing a operating condition of the memory, wherein the operating condition includes one or more of a supply voltage, a reference voltage and temperature, and repeating the transmitting steps and performing with the changed operating condition present. However, it would have been obvious design choice to a person of ordinary skill in the art, at the time the invention was made, to change an operating condition of the memory, wherein the operating condition includes one or more of a supply voltage, a reference voltage and temperature, and repeating the transmitting steps and performing with the changed operating condition present so that during these operations, DLL can be monitored to observe its behavior due to changes in the power supply caused by the operation or due to changes in operating conditions such as voltage or temperature, or both.

6. Applicant's arguments with respect to claims 1-2, 4-7 and 9-15 are moot in view of the new ground(s) of rejection.

Note applicant's argument with respect to Silvestri (6,385,129) that Silvestri does not teach or disclose a serial presence detect circuit containing a plurality of test bits.

However, Cranford, Jr. et al (US 2005/0111536) disclose a serial presence detect circuit containing a plurality of test bits (an integrated transmission chip (1) may comprise an internal build-in self test unit BIST (1.6) which is able to generate a pseudo random bit sequence PRBS. This bit

sequence can be used for further tests). (See paragraph (0066)). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the serial presence detect circuit containing a plurality of test bits (an integrated transmission chip (1) may comprise an internal build-in self test unit BIST (1.6) which is able to generate a pseudo random bit sequence PRBS. This bit sequence can be used for further tests) as taught by Cranford, Jr. et al into the memory chip of Silvestri so that it can be able to generate a pseudo random bit sequence PRBS which can be used for further tests. Therefore, with the combination of Silvestri and Cranford, Jr. et al, their system can perform the method steps as claimed by the instant application. 9See the above rejection).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHUNG My CHUNG whose telephone number is (571)272-3818. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Phung My Chung/
Primary Examiner
Art Unit 2117